THAT WHICH IS CLAIMED IS:

1. A memory device comprising:

a capacitor comprising a lower electrode, an upper electrode and a dielectric layer interposed between the lower electrode and the upper electrode; and

a multi-layered encapsulating layer surrounding the capacitor, the multi-layered encapsulating layer comprising a first blocking layer which is annealed and a first protection layer formed on the annealed first blocking layer, the first blocking layer and the first protection layer being formed of the same material.

2. The memory device of claim 1, wherein the first blocking layer has an enough thickness to block diffusion of hydrogen generated during the formation of the first protection layer.

3. The memory device of claim 1, wherein the first blocking layer is a metallic oxide layer.

4. The memory device of claim 2, wherein the first blocking layer is a metallic oxide layer.

5. The memory device of claim 3, wherein the metallic oxide layer is formed of one selected from the group consisting of Al_2O_3, TiO_2, ZrO_2, Ta_5O_3 and CeO_2.

6. The memory device of claim 1, wherein the thickness of the first blocking layer is 10-50% of the thickness of the first protection layer.

7. The memory device of claim 6, wherein the first blocking layer is formed of Al_2O_3.

8. The memory device of claim 7, wherein the thickness of the first blocking layer is 10-15 Å, and the thickness of the first protection layer is about 100 Å.

9. The memory device of claim 1, wherein the first blocking layer and the first protection layer are formed by an atomic layer deposition method, a low pressure chemical vapor deposition method, a high pressure chemical vapor deposition method or a plasma chemical vapor deposition method.

10. The memory device of claim 1, further comprising an interlayer insulation layer formed on the first protection layer and a second encapsulating layer formed on the interlayer insulation layer, the second encapsulating layer comprising a second blocking layer which is annealed and a second protection layer formed on the second blocking layer, the second blocking layer and the second protection layer comprising the same material.

11. The memory device of claim 10, wherein the second blocking layer has an enough thickness to block diffusion of hydrogen generated during the formation of the second protection layer.

12. The memory device of claim 10, wherein the second blocking layer is a metallic oxide layer.

13. The memory device of claim 11, wherein the second blocking layer is a metallic oxide layer.

14. The memory device of claim 12, wherein the metallic oxide layer is formed of one selected from the group consisting of Al_2O_3, TiO_2, ZrO_2, Ta_5O_3 and CeO_2.

15. A memory device comprising:

a lower electrode;

a dielectric layer formed on a predetermined portion of the surface of the lower electrode;

a spacer layer formed on the lower electrode, the spacer layer comprising a blocking spacer directly contacting a sidewall of the dielectric layer and a protection spacer formed on the blocking spacer;

an interlayer insulation layer formed on the lower electrode to contact the protection spacer;

an upper electrode formed on the dielectric layer; and

a multi-layered encapsulating layer surrounding the interlayer insulation layer, the spacer layer and the upper electrode, the multi-layered encapsulating layer comprising a first blocking layer which is annealed and a first protection layer formed on the annealed first blocking layer, the first blocking layer and the first protection layer being formed of the same material.

16. The memory device of claim 15, wherein the first blocking layer has an enough thickness to block diffusion of hydrogen generated during the formation of the first protection layer.

17. The memory device of claim 15, wherein the first blocking layer is a metallic oxide layer.

18. The memory device of claim 16, wherein the first blocking layer is a metallic oxide layer.

19. The memory device of claim 17, wherein the metallic oxide layer is formed of one selected from the group consisting of Al_2O_3, TiO_2, ZrO_2, Ta_5O_3 and CeO_2.

20. The memory device of claim 16, wherein the first blocking layer is formed of Al_2O_3.

21. The memory device of claim 20, wherein the thickness of the first blocking layer is 10-15 Å, and the thickness of the first protection layer is about 100 Å.

22. The memory device of claim 15, wherein the first blocking layer and the first protection layer are formed by an atomic layer deposition method, a low pressure chemical vapor deposition method, a high pressure chemical vapor deposition method or a plasma chemical vapor deposition method.

23. The memory device of claim 15, further comprising a second interlayer insulation layer formed on the first protection layer and a second encapsulating layer formed on the second interlayer insulation layer, the second encapsulating layer comprising a second blocking layer which is annealed and a second protection layer formed on the second blocking layer, the second blocking layer and the second protection layer comprising the same material.

24. The memory device of claim 23, wherein the second blocking layer has sufficient thickness to block diffusion of hydrogen generated during the formation of the second protection layer.

25. The memory device of claim 23, wherein the second blocking layer is a metallic oxide layer.

26. The memory device of claim 24, wherein the second blocking layer is a metallic oxide layer.

27. The memory device of claim 25, wherein the metallic oxide layer is formed of one selected from the group consisting of Al_2O_3, TiO_2, ZrO_2, Ta_5O_3 and CeO_2.

28. The memory device of claim 15, wherein the blocking spacer has an enough thickness to block diffusion of hydrogen generated during the formation of the protection spacer.

29. The memory device of claim 15, wherein the blocking spacer is a metallic oxide layer.

30. The memory device of claim 28, wherein the blocking spacer is a metallic oxide layer.

31. The memory device of claim 30, wherein the metallic oxide layer is formed of one selected from the group consisting of Al_2O_3, TiO_2, ZrO_2, Ta_5O_3 and CeO_2.

32. An integrated circuit, comprising:

a ferroelectric dielectric region on a substrate;

a first metal oxide layer directly on a surface of the ferroelectric dielectric region; and

a second metal oxide layer on the first metal oxide layer,

wherein the first metal oxide layer is configured to enable a remnant polarization of the ferroelectric dielectric region to increase during an annealing of the substrate before formation of the second metal oxide layer.

33. An integrated circuit according to Claim 32, wherein the first metal oxide layer is thick enough to substantially impede diffusion of hydrogen into the ferroelectric dielectric region.

34. An integrated circuit according to Claim 32:

wherein the first metal oxide layer comprises a metal oxide selected from the group consisting of Al_2O_3, TiO_2, ZrO_2, Ta_5O_3 and CeO_2; and

wherein the second metal oxide layer comprises a metal oxide selected from the group consisting of Al_2O_3, TiO_2, ZrO_2, Ta_5O_3 and CeO_2.

35. An integrated circuit according to Claim 32, wherein the second metal oxide layer is thicker than the first metal oxide layer.

36. An integrated circuit according to Claim 35, wherein the second metal oxide layer is at least about twice as thick as the first metal oxide layer.

37. An integrated circuit according to Claim 36, wherein the second metal oxide layer is less than about ten times as thick as the first metal oxide layer.

38. An integrated circuit according to Claim 35, wherein the first and second metal oxide layers each are Al_2O_3 layers.

39. An integrated circuit according to Claim 38, wherein the first metal oxide layer has a thickness in range from about 10 Å to about 15 Å and wherein the second metal oxide layer has a thickness greater than about 50 Å.

40. An integrated circuit according to Claim 32, wherein the ferroelectric dielectric region is a dielectric of a capacitor.

41. An integrated circuit according to Claim 32, wherein the ferroelectric dielectric region comprises a ferroelectric material selected from the group consisting of $SrTiO_3$, $BaTiO_3$, (Ba, Sr)TiO_3, Pb(Zr, Ti)O_3, $SrBi_2Ta_2O_9$, (Pb, La)(Zr, Ti)O_3 and $Bi_4Ti_3O_{12}$.

42. A method of manufacturing a memory device, comprising the steps of:

forming a capacitor on a semiconductor substrate, the capacitor comprising a lower electrode, an upper electrode and a dielectric layer interposed between the lower electrode and the upper electrode; and

forming a multi-layered encapsulating layer to surround the capacitor, the multi-layered encapsulating layer comprising a first blocking layer which is annealed and a first protection layer formed on the first blocking layer, the first blocking layer and the first protection layer being formed of the same material.

43. The method of claim 42, wherein in the step of forming the multi-layered encapsulating layer, the first blocking layer is formed to have an enough thickness to block diffusion of hydrogen generated during the formation of the first protection layer.

44. The method of claim 42, wherein the first blocking layer and the first protection layer are formed by an atomic layer deposition method, a low pressure chemical vapor deposition method, a high pressure chemical vapor deposition method, a plasma chemical vapor deposition method or a chemical vapor deposition method.

45. The method of claim 42, wherein the first blocking layer is a metallic oxide layer.

46. The method of claim 45, wherein the metallic oxide layer is formed of one selected from the group consisting of Al_2O_3, TiO_2, ZrO_2, Ta_5O_3 and CeO_2.

47. The method of claim 42, wherein in the step of forming the multi-layered encapsulating layer, the thickness of the first blocking layer is 10-50% of the thickness of the first protection layer.

48. The method of claim 47, wherein the first blocking layer is formed of Al_2O_3.

49. The method of claim 48, wherein the thickness of the first blocking layer is 10-15 Å, and the thickness of the first protection layer is about 100 Å.

50. The method of claim 42, wherein the step forming the multi-layered encapsulating layer comprises the step of annealing the first protection layer after the first protection layer is formed.

51. The method of claim 42, further comprising the steps of forming an interlayer insulation layer on the multi-layered encapsulating layer and forming a second multi-layered encapsulating layer on the interlayer insulation layer, the second multi-layered encapsulating layer comprising a second blocking layer which is annealed and a second protection layer formed on the second blocking layer, the second blocking layer and the second protection layer being formed of the same material, after the step of forming the multi-layered encapsulating layer.

52. The method of claim 51, wherein in the step of forming the second multi-layered encapsulating layer, the second blocking layer is formed to have an enough thickness to block diffusion of hydrogen generated during the formation of the second protection layer.

53. The method of claim 51, wherein the second blocking layer is a metallic oxide layer.

54. The method of claim 53, wherein the metallic oxide layer is formed of one selected from the group consisting of Al_2O_3, TiO_2, ZrO_2, Ta_5O_3 and CeO_2.

55. The method of claim 53, wherein the second blocking layer and the second protection layer are formed by an atomic layer deposition method, a low pressure chemical vapor deposition method, a high pressure chemical vapor deposition method or a plasma chemical vapor deposition method.

56. The method of claim 51, further comprising the step of annealing the second protection layer after the step of forming the second protection layer of the second multi-layered encapsulating layer.

57. The method of claim 42, wherein the step of forming the capacitor comprises the steps of: forming the lower electrode on the semiconductor substrate; forming an interlayer insulation layer on the entire surface of the semiconductor substrate, the interlayer insulation layer including a contact hole exposing a predetermined portion of the lower electrode; forming a spacer layer on each sidewall of the contact hole using a single material, the spacer layer comprising a blocking spacer which is annealed; forming the dielectric layer by filling the contact hole limited by the spacer layer with dielectric; and forming the upper electrode on the surface of the dielectric layer.

58. A method of forming a protective structure for a ferroelectric dielectric region on an integrated circuit substrate, the method comprising:

depositing a first metal oxide layer directly on a surface of the ferroelectric dielectric region;

annealing the first metal oxide layer and the ferroelectric dielectric region; and

depositing a second metal oxide layer on the first metal oxide layer.

59. A method according to Claim 58, wherein the first metal oxide layer is sufficiently thin enough to enable a remnant polarization of the ferroelectric dielectric region to increase during the annealing of the first metal oxide layer and the ferroelectric dielectric region.

60. A method according to Claim 58, wherein annealing the first metal oxide layer and the ferroelectric dielectric region comprises annealing the first metal oxide layer and the ferroelectric dielectric region in a manner sufficient to increase the remnant polarization of the ferroelectric dielectric region.

61. A method according to Claim 58, wherein the first metal oxide layer is sufficiently thick enough to reduce diffusion of hydrogen into the dielectric region during the depositing of the second metal oxide layer.

62. A method according to Claim 58:

wherein the first metal oxide layer comprises a metal oxide selected from the group consisting of Al_2O_3, TiO_2, ZrO_2, Ta_5O_3 and CeO_2; and

wherein the second metal oxide layer comprises a metal oxide selected from the group consisting of Al_2O_3, TiO_2, ZrO_2, Ta_5O_3 and CeO_2.

63. A method according to Claim 58, wherein the second metal oxide layer is thicker than the first metal oxide layer.

64. A method according to Claim 63, wherein the second metal oxide layer is at least about twice as thick as the first metal oxide layer.

65. A method according to Claim 64, wherein the second metal oxide layer is less than about ten times as thick as the first metal oxide layer.

66. A method according to Claim 63:

wherein depositing a first metal oxide layer comprises depositing a first Al_2O_3 layer; and

wherein depositing a second metal oxide layer comprises depositing a second Al_2O_3 layer.

67. A method according to Claim 66, wherein the first Al_2O_3 layer has thickness in a range from about 10 Å to about 15 Å, and wherein the second Al_2O_3 layer has a thickness greater than about 50 Å.

68. A method according to Claim 67:

wherein depositing a first Al_2O_3 layer comprises depositing the first Al_2O_3 layer at a temperature of about 500 °C in an oxygen atmosphere;

wherein annealing the first metal oxide layer and the ferroelectric dielectric region comprises annealing the first Al_2O_3 layer at a temperature in a range from about 400 °C to about 600 °C; and

wherein depositing a second Al_2O_3 layer comprises depositing the second Al_2O_3 layer at a temperature of about 500 °C in an oxygen atmosphere.

69. A method according to Claim 68, further comprising annealing the second Al_2O_3 layer.

70. A method according to Claim 58:

wherein depositing a first metal oxide layer comprises depositing the first metal oxide layer according to one of an atomic layer deposition method, a low pressure chemical vapor deposition method, a high pressure chemical vapor deposition method, a plasma chemical vapor deposition method or a chemical vapor deposition method; and

wherein depositing a second metal oxide layer comprises depositing the second metal oxide layer according to one of an atomic layer deposition method, a low pressure chemical vapor deposition method, a high pressure chemical vapor deposition method, a plasma chemical vapor deposition method or a chemical vapor deposition method

71. A method according to Claim 58, wherein the ferroelectric dielectric region is a capacitor dielectric.

72. A method according to Claim 58, wherein the ferroelectric dielectric region comprises a ferroelectric material selected from the group consisting of $SrTiO_3$, $BaTiO_3$, $(Ba, Sr)TiO_3$, $Pb(Zr, Ti)O_3$, $SrBi_2Ta_2O_9$, $(Pb, La)(Zr, Ti)O_3$ and $Bi_4Ti_3O_{12}$.